REMARKS

Claim 16 calls for a semiconductor substrate and a layer of chalcogenide material over the substrate.

In paragraph 3 of the final rejection, it is asserted that the claim is anticipated by Ichihara. This is so contended because it is claimed that the layer 102 may be formed of silicon.

It is respectfully submitted that this position is based on a misreading of the reference. Nowhere in the reference does it ever in any way suggest that the layer 102 is silicon. To the contrary, the layer 102 is described in connection with Figure 2. See paragraph 119. This is one embodiment of the present invention. The material cited for the teaching of a semitransparent layer that is possibly including silicon is at paragraph 214 which is under a second example. See the heading above 194. Thus, it is clear that paragraph 214 is a totally different embodiment. In fact, paragraph 214 is talking about a different embodiment than the second example at 194.

As explained in paragraph 213, the example of paragraph 194 *et seq.* called the second example, is a four layer structure as shown in Figure 7. It is suggested in paragraph 213 that in another embodiment a five layer structure may be used "wherein an Au semitransparent film is provided in the four layer structure." Thus, the reference in 214 to a semitransparent layer is not a reference to the semitransparent layer in the different embodiment of Figure 2, but, rather, to the semitransparent in the five layer alternative structure, the alternative being to the embodiment of the second example. In other words, the Examiner has misread the semitransparent layer referred to in 214 to be the semitransparent layer in the embodiment of Figure 2. There is no basis for this reading.

To the contrary, the semitransparent layer is the fifth layer of a five layer structure which is nowhere shown. Nor does the reference ever suggest where this fifth layer is placed. Thus, we do not know if it could constitute a layer under the chalcogenide material or whether it would be over the chalcogenide material. The reference is simply silent on the point. Therefore, reconsideration would be appropriate.

Further, with respect to the rejection of claim 23, based on Horie, the rationale for the combination is not clear. The embodiment relied upon in Horie is one in which a conventional semiconductor phase change memory is utilized. But this embodiment in no way suggests any reason to use a layer of chalcogenide material over a semiconductor substrate where the

chalcogenide material includes a species to reduce the grain size of the chalcogenide material and a species to increase the crystallization speed. In other words, there is no teaching of any reason to make these changes in a semiconductor phase change memory, as opposed to an optical disk.

The assertion, with respect to both Mizuuchi and Ichihara, that functional limitations may be ignored is improper and is directly rebutted by the Manual of Patent Examining Procedure as recently amended. See M.P.E.P. § 2173.05(G). There, it is explained that members adapted to be positioned define structural attributes of the interrelated components, citing *In re Venezia*. In other words, the components must be so configured because the claimed increase in crystallization speed and reduction in grain size. As explained in § 2173.05(G), there is nothing wrong with defining an invention in functional terms. "A functional limitation must be evaluated and considered, just like any other limitation to claim for what it fairly conveys to a person of ordinary skill ... ." Thus, it is clear that these are proper limitations and that they are not taught by Horie. As a result, there is no reason to believe that any cited reference suggests any reason to apply the claimed arrangement in a semiconductor memory which includes a semiconductor substrate and a chalcogenide material over that substrate. Moreover, the cited references do not even teach the claimed functions.

Therefore, reconsideration of the rejections of claims 16 and 23 based on Ichihara or Mizuuchi is requested.

With respect to claim 24, it was previously pointed out that it does not appear that any titanium containing layer is under the chalcogenide material in Mizuuchi. For example, in connection with Figure 2 of the Mizuuchi layer, the recording layer 4 and the layer suggested to have the titanium as the layer 3, clearly above the recording layer. Likewise, in Figure 2, the reflective layer 106 is over the recording layer 105 in Ichihara. Thus, it is again requested that this rejection be reconsidered.

The suggestion that the preamble need not be given weight in calling for a semiconductor does not address the fact that claim 16, in its body, also recites a semiconductor substrate.

In view of these remarks, reconsideration is requested.

Respectfully submitted,

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